

AMENDMENTS TO THE CLAIMS ARE AS FOLLOWS:

What is claimed is:

- 1) (CURRENTLY AMENDED). A method of fabricating a ~~semiconductor~~ MOSFET device with shallow source/drain extension junctions comprising the steps:
 - forming a pre-amorphized implant layer in between shallow trench isolation regions and adjacent to gate electrode structure on a semiconductor substrate;
 - performing ion implantation of dopants in said pre-amorphized implant layer to form source/drain extension regions; and
 - performing a sequential dual step annealing of said source/drain extension regions comprising:
 - a) a first low energy multiple-pulse laser anneal step in the sub-melt regime to activate the dopants in the source/drain extension regions followed by
 - b) a second rapid thermal anneal step to heal residual damage from the ion implantation and to cause the out-diffusion of the dopants in the source/drain extension regions to yield shallower source/drain extension junctions than the just-implanted source/drain extensions.
- 2) (CURRENTLY AMENDED). The method of fabricating a ~~semiconductor~~ MOSFET device according to claim 1, wherein said pre-amorphitization implantation is done with ions comprising Ge^+ or Si^+ .
- 3) (CURRENTLY AMENDED). The method of fabricating a ~~semiconductor~~ MOSFET

device according to claim 2, wherein said Ge^+ or Si^+ ion implant ion energy is approximately between 1 keV and 20 keV and the dose is approximately between $1\text{E}14$ and $1\text{E}16$ ions/ cm^2 .

4) (CURRENTLY AMENDED). The method of fabricating a ~~semiconductor~~ MOSFET device according to claim 1, wherein said SDE implant is done with B^+ ions.

5) (CURRENTLY AMENDED). The method of fabricating a ~~semiconductor~~ MOSFET device according to claim 4, wherein said B^+ ion implant energy is approximately between 0.2 keV and 0.7 keV and the dose is approximately between $5\text{E}14$ and $1\text{E}16$ ions/ cm^2 .

Claims 6 and 7 are cancelled.

8) (CURRENTLY AMENDED). The method of fabricating a semiconductor device according to claim ~~7~~ 1, wherein said laser ~~irradiation~~ anneal is done using a multiple-pulsed 248 nm KrF excimer laser beam.

9) (PREVIOUSLY PRESENTED). The method of fabricating a semiconductor device according to claim 8, wherein said laser beam has a fluence of approximately between $0.1 \text{ J}/\text{cm}^2$ and $0.4 \text{ J}/\text{cm}^2$, pulse duration of approximately between 10 nsec and 40 nsec, and a repetition rate of 1 – 1000 pulses.

10) (CURRENTLY AMENDED). The method of fabricating a semiconductor device according to claim ~~6~~ 1, wherein said rapid thermal anneal is done at approximately between 800

°C and 1200 °C for a duration of approximately between 0 sec and 60 sec.

11) (CURRENTLY AMENDED). A method of fabricating a MOSFET device with shallow source/drain extension junctions comprising the steps:

forming a pre-amorphized Ge^+ or Si^+ implant layer in between shallow trench isolation regions and adjacent to gate electrode structure on a silicon substrate;

performing B^+ ion implantation of dopants in said pre-amorphized implant layer to form source/drain extension regions; and

performing a sequential dual step annealing of said source/drain extension regions comprising ~~low temperature sub-melt regime laser anneal and rapid thermal anneal~~ :

a) a first low energy multiple-pulse laser anneal step in the sub-melt regime to activate the dopants in the source/drain extension regions followed by

b) a second rapid thermal anneal step to heal residual damage from the ion implantation and to cause the out-diffusion of the dopants in the source/drain extension regions to yield shallower source/drain extension junctions than the just-implanted source/drain extensions.

12) (PREVIOUSLY PRESENTED). The method of fabricating a MOSFET device with shallow source/drain extension junctions according to claim 11, wherein said Ge^+ or Si^+ ion implant ion energy is approximately between 1 keV and 20 keV and the dose is approximately between $1\text{E}14$ and $1\text{E}16$ ions/ cm^2 .

13) (PREVIOUSLY PRESENTED). The method of fabricating a MOSFET device with shallow source/drain extension junctions according to claim 11, wherein said B^+ ion implant

energy is approximately between 0.2 keV and 0.7 keV and the dose is approximately between 5×10^{14} and 1×10^{16} ions/cm².

14) (CURRENTLY AMENDED). The method of fabricating a MOSFET device with shallow source/drain extension junctions according to claim 11, wherein said low ~~temperature~~ energy laser anneal is done using a multiple-pulsed 248 nm KrF excimer laser ~~so as not to melt said pre-amorphized implant layer.~~

15) (PREVIOUSLY PRESENTED). The method of fabricating a MOSFET device with shallow source/drain extension junctions according to claim 14, wherein said multiple-pulsed laser beam has a fluence of approximately between 0.1 J/cm² and 0.4 J/cm², pulse duration of approximately between 10 nsec and 40 nsec, and a repetition rate of 1 – 1000 pulses.

16) (PREVIOUSLY PRESENTED). The method of fabricating a MOSFET device with shallow source/drain extension junctions according to claim 11, wherein said rapid thermal anneal is done at approximately between 800 °C and 1200 °C for a duration of approximately between 0 sec and 60 sec.

17) (CURRENTLY AMENDED). A method of forming shallow source/drain extension junctions in a MOSFET device, comprising the steps:

performing B⁺ ion implantation of dopants in a pre-amorphized implant layer to form source/drain extension regions on a silicon substrate; and

performing a sequential dual step annealing of said source/drain extension regions

comprising ~~low temperature sub-melt regime laser anneal and rapid thermal anneal~~ ;

a) a first low energy multiple-pulse laser anneal step in the sub-melt regime to activate the dopants in the source/drain extension regions followed by

b) a second rapid thermal anneal step to heal residual damage from the ion implantation and to cause the out-diffusion of the dopants in the source/drain extension regions to yield shallower source/drain extension junctions than the just-implanted source/drain extensions.

18) (PREVIOUSLY PRESENTED). The method of forming shallow source/drain extension junctions in a MOSFET device according to claim 17, wherein said B⁺ ion implant energy is approximately between 0.2 keV and 0.7 keV and the dose is approximately between 5E14 and 1E16 ions/cm².

19) (CURRENTLY AMENDED). The method of forming shallow source/drain extension junctions in a MOSFET device according to claim 17, wherein said low ~~temperature~~ energy laser anneal is done using a multiple-pulsed 248 nm KrF excimer laser ~~so as not to melt said pre-amorphized implant layer.~~

20) (PREVIOUSLY PRESENTED). The method of forming shallow source/drain extension junctions in a MOSFET device according to claim 19, wherein said multiple-pulsed laser beam has a fluence of approximately between 0.1 J/cm² and 0.4 J/cm², pulse duration of approximately between 10 nsec and 40 nsec, and a repetition rate of 1 – 1000 pulses.

21) (PREVIOUSLY PRESENTED). The method of forming shallow source/drain

extension junctions in a MOSFET device according to claim 17, wherein said rapid thermal anneal is done at approximately between 800 °C and 1200 °C for a duration of approximately between 0 sec and 60 sec.

22) (CURRENTLY AMENDED). A method of forming a MOSFET device with shallow source/drain extension junctions, comprising the steps:

forming shallow trench isolation regions on a silicon substrate;

forming the gate stack in between said shallow trench isolation regions;

removing the sidewall spacers from around said gate stack;

forming a pre-amorphized Ge^+ or Si^+ implant layer in silicon, between shallow trench isolation regions and adjacent to gate electrode structure;

performing B^+ ion implantation of dopants in said pre-amorphized implant layer to form source/drain extension regions; and

performing a sequential dual step annealing of said source/drain extension regions comprising: ~~low temperature multiple pulsed laser anneal and rapid thermal anneal. So as to not melt said pre-amorphized implant layer.~~

a) a first low energy multiple-pulse laser anneal step in the sub-melt regime to activate the dopants in the source/drain extension regions followed by

b) a second rapid thermal anneal step to heal residual damage from the ion implantation and to cause the out-diffusion of the dopants in the source/drain extension regions to yield shallower source/drain extension junctions than the just-implanted source/drain extensions.

23) (PREVIOUSLY PRESENTED). The method of forming a MOSFET device with

shallow source/drain extension junctions according to claim **22**, wherein said Ge^+ or Si^+ ion implant ion energy is approximately between 1 keV and 20 keV and dose is approximately between $1\text{E}14$ and $1\text{E}16$ ions/ cm^2 .

24) (PREVIOUSLY PRESENTED). The method of forming a MOSFET device with shallow source/drain extension junctions according to claim **22**, wherein said B^+ ion implant energy is approximately between 0.2 keV and 0.7 keV and the dose is approximately between $5\text{E}14$ and $1\text{E}16$ ions/ cm^2 .

25) (CURRENTLY AMENDED). The method of forming a MOSFET device with shallow source/drain extension junctions according to claim **22**, wherein said multiple-pulsed laser ~~beam~~ anneal step is done using a 248 nm KrF excimer laser with a fluence of approximately between 0.1 J/cm^2 and 0.4 J/cm^2 , pulse duration of approximately between 10 nsec and 40 nsec, and a repetition rate of 1 – 1000 pulses.

26) (PREVIOUSLY PRESENTED). The method of forming a MOSFET device with shallow source/drain extension junctions according to claim **22**, wherein said rapid thermal anneal is done at approximately between 800°C and 1200°C for a duration of approximately between 0 sec and 60 sec.